

REMARKS

Claims 1 to 20 are pending in this application, of which claims 1, 8, and 16 are independent. Favorable reconsideration and further examination are respectfully requested.

Initially, we thank the Examiner for the courtesies extended during a telephone interview held on April 14, 2010. No agreement was reached during that interview.

In the November 9, 2010 Office Action, all of the claims were rejected over U.S. Patent No. 5,339,275 (Hyatt). As shown above, the claims have been amended.

Independent claim 1 recites:

1. A controller comprising:
a control circuit comprising a closed loop circuit, the closed loop circuit comprising:
 an input;
 an output;
 a forward path coupled to the input and to the output;
 a feedback path coupled to the input and to the output; and
 a sensor having a sensitivity, the sensor being in the forward path or in the feedback path, the sensor for generating a sensor signal;
 an error signal generator that is external to the closed loop circuit, the error signal generator to generate an error signal and to provide the error signal to the closed loop circuit such that the error signal is incorporated into a useful signal of the closed loop circuit, wherein the error signal is predetermined, the closed loop circuit being configured to generate an output signal at an output of the closed loop circuit, the output signal being based on the sensor signal and the error signal, the output signal being sent along the feedback path to the input of the control circuit; and
 a detector configured to detect a change in the sensitivity of the sensor, the detector being coupled to the forward path, the detector to generate a control signal;
 wherein the forward path comprises a control device, which is coupled to the output, to limit an output signal at the output to a predetermined value, the detector to control the control device using the control signal.

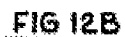
The applied art is not understood to disclose at least the underlined features of claim 1 above.

In this regard, the Office Action equates circuit 996 of Fig. 12B to the claimed control circuit and, apparently, the circuit of Fig. 5 to the claimed forward and feedback paths. In

Fig. 5. Regarding its Figs. 5 and 12B, as previously explained, Hyatt states

The circuits shown in FIG. 12B will now be discussed for the embodiment of the reverberation unit of FIG. 5, wherein input signal 504 (FIG. 5) may be the same as analog input signal AI 504 (FIG. 12B) and output signal 507 (FIG. 5) may be the same as analog output signal 507 (FIG. 12B) and wherein register 501 (FIG. 5) may include CCD memory 932, refresh circuit 996, and the other circuitry [sic] shown in FIG. 12B. In a preferred embodiment, the analog refresh arrangement of the present invention may be used with the reverberation circuit of FIG. 5 as shown in FIG. 12B. For simplicity of discussion, it will be assumed that clock 943 is a one MHz clock, that CCD memory 932 is a 100 stage shift register, and that analog input AI 504 is sampled and output sample 507 is generated for each recirculation of CCD memory 932; yielding an input and output rate of 10 KHz. This is based upon one input and output sample every 100 clock pulses, which is once per recirculation of CCD memory 932.² (emphasis added)

² Col. 104, line 59 to col. 105, line 9



The diagram shows a control logic circuit. An input M1 is connected to an AND gate 386 and an OR gate 388. The output of AND gate 386 goes to a transistor 391. The output of OR gate 388 goes to an AND gate 387 and another transistor 392. The output of AND gate 387 goes to a transistor 347. The outputs of transistors 391 and 347 are connected to a common bus 390. This bus 390 is also connected to the input of a refresh circuit 396. The refresh circuit 396 has a feedback loop from its output back to its input. The output of the refresh circuit 396 is connected to a counter 393 via line 394. The counter 393 is connected to a decoder 395 via line 395. The decoder 395 has multiple outputs, one of which is labeled 399. There are also other signal lines like 391, 347, 392, 393, 394, 395, 396, 397, 398, and 399 shown throughout the circuit.

Thus, we assume that register 501 of Fig. 5 may include refresh circuit 996 (the alleged counterpart to the claimed control circuit³). Assuming that these are the connections relied upon in the Office Action, we do not understand how a sensor would be incorporated into the circuitry depicted in Figs. 5, 9F and 12.

In this regard, the Office Action continues to allege that the transducer mentioned at column 116, lines 56 to 61 of Hyatt corresponds to the claimed sensor. That portion of Hyatt is reproduced below:

The term signal is herein intended to include electrical signals, charge signals, current signals, acoustic signals, illumination signals, magnetostrictive signals, sonic signals, magnetic signals, and other known signals which may be sensed such as with a transducer and which may be processed such as with a filter.

As previously explained, this portion of Hyatt merely describes how the word “signal” is defined. It is not describing the transducer itself, much less how such a transducer would fit in connection with the remaining circuitry described in Hyatt (much less the circuitry of Figs. 5, 9F or 12B) or how that transducer would operate.

During the interview, the Examiner appeared to explain that this portion of Hyatt implies use of a sensor and, consequently, suggests the claimed sensor. We respectfully disagree with this contention. However, even if this were true⁴, we do not understand this portion of Hyatt to disclose or to suggest that the sensor is in a forward path or in a feedback path of a closed loop control circuit. That is, in the following excerpt on page 3, the Office Action alleges the existence of a forward or feedback path in Fig. 5 and the existence of a sensor.

³ Office Action, page 3

⁴ We do not concede that this is true, but assume truth merely for the sake of argument.

a sensor (e.g., filter, register 501) (see Col. 116, Lines 56-61), which is in the forward path or in the feedback path (see Figure 5 and 12B), the sensor for generating a sensor signal (e.g., magnetostrictive signals) (see Col. 116, Lines 56-61);

Yet, there is no explanation in the Office Action (much less disclosure in the reference) as to why there would be a sensor in the alleged feedback of feedforward paths of Fig. 5. In this regard, we note that the following excerpt of column 19 of Hyatt was relied upon on page 3 of the Office Action for its disclosure of feedback and feedforward paths:

Input signals 504 and 505 and output signals 506 and 35
507 may be interconnected for feedforward and/or
feedback operations. For example, an output signal 506
having a first time delay may be connected to an input
signal 505 having a second time delay. If the first time
delay is greater than the second time delay, then a feed-
back connection is provided. If the second time delay is 40
greater than the first time delay, then a feedforward
connection is provided.

We do not see where, in the paths identified in this paragraph, it would be beneficial, much less appropriate, to incorporate a sensor of the type claimed. We also do not understand these paths to constitute closed loop control circuits, again as claimed.

Regarding the claimed detector, on page 4, the Office Action relies upon detectors 643 and 645, as follows:

a detector (e.g., detectors 643 and 645), which is coupled to the forward path (e.g., used in conjunction with CCD memory), to obtain an intermediate signal from the forward path between the input and the output, the detector for generating a control signal (see Col. 82, Lines 34-44; and Figure 12B);

As previously noted, Hyatt states “[d]igital detector circuits 643 and 645 have been discussed as digital detectors with reference to FIG. 6D.”⁵ However, nowhere are these detectors shown. In fact, Fig. 6D is a flowchart showing a computer subroutine, not a sensor that could be in the forward path or in the feedback path, as claimed. Consequently, we do not understand there to be any disclosure or suggestion to incorporate detectors into the circuitry of Figs. 5, 9F or 12B in the manner claimed.

Even if one were to assume that detector circuits 643 and 645 could somehow be incorporated in to the circuitry of Figs. 5, 9F or 12B (a point that we do not concede), nowhere does Hyatt disclose or suggest that its detector circuits perform the function of the claimed detector, namely to detect a change in the sensitivity of the sensor, and to generate a control signal. In this regard, referring to Fig. 6D, column 82 of Hyatt states:

The arrangement discussed with reference to FIG. 6D may also be implemented with a CCD register embodiment. For example, trace signal T may be processed with an operational amplifier 623 to provide input signal samples T_L . Sample device 624 may be a well known sample-and-hold circuit as discussed with reference to sample-and-hold 777 (FIG. 7E). Alternately, sample circuit 624 may be eliminated. P-ROM 625 may store single-bit digital signal samples for gating trace signal sample T_L in response to a one-state pilot signal sample and for not gating trace signal sample T_L in response to a zero-state pilot signal sample from P-ROM 625. Product circuit 626 may be a single FET switch as discussed with reference to FIG. 4 above for either gating or not gating the input analog trace signal samples to be summed into the output signal sample memory. Z-RAM 614 and Z-counter 613 may be replaced with a CCD memory for storing analog signal samples from product circuit 626 as discussed for a CCD embodiment with reference to FIG. 4 above and as discussed for compositor 903 with reference to FIG. 9E above. Digital detector circuits 643 and 645 have been discussed as digital detectors with reference to FIG. 6D.

⁵ Col. 82, lines 34 to 36.

Alternately, detectors 643 and 645 may be implemented as analog detectors such as Schmidt triggers or other analog threshold detectors for an analog output signal sample embodiment. Control circuitry including compositor control 632, one-shot 651, counters 616-619, decoder 622, and decoder 628 which have been discussed above for a digital embodiment but may also be used in conjunction with the analog or hybrid CCD memory embodiment.⁶

This is the only place that detectors 643 and 645 are described, and Fig. 6D, with which they are described, does not even show the detectors. Consequently, we do not believe that the detectors can properly be equated to the claimed detector.

For at least the foregoing reasons, claim 1 is believed to be patentable over Hyatt.

Independent claims 8 and 16 are likewise believed to be patentable.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing remarks, the entire application is now believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

⁶ Col. 82, lines 13 to 44

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Please apply any deficiency in fees or credit any overpayment to deposit
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Respectfully submitted,

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